REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed January 12, 2005. Claims 1-38 remain pending in this application. Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102 & 103

Claims 1-38 stand rejected as anticipated by U.S. Patent No. 5,651,123 ("Nakagawa") or as obvious over Nakagawa in view of U.S. Patent No. 5,490,280 ("Gupta"), U.S. Patent No. 5,530,837 ("Williams") or U.S. Patent No. 6,389,562 ("Kondo"). Applicant respectfully traverses these rejections.

Independent Claims 1, 20, 31 and 38

Claim 1 recites "an apparatus for allocating one or more resources within a processor to an instruction, the apparatus comprising: a sequence generator that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the resources within the processor, and a resource identifier selector coupled to the sequence generator, the resource identifier selector selecting one or more of the resource identifiers for allocation to the instruction." Claims 20, 31 and 38 recite similar limitations.

The Examiner states in the Official Action that the claim language "resources within a processor" as used in Claim 1 is interpreted as "any processing source in a data processing system, such as instructions stored in a specific memory address based on Applicant's own disclosure" and cites Page 3, Lines 11-20. Applicant respectfully disagrees with this assessment. After reviewing the portions of the Background of the Invention cited by the Examiner, Applicant cannot find where this passage indicates processing sources in a data processing system. The portion cited by the Examiner is in the Background of the Invention section which is specifically "described in connection with microprocessor resource allocators" (*See* Page 3, Line 2). Thus, the hardware structures, such as buffers, referred to at Page 3, Lines 11-20 are resources within a processor.

The term processor as is known in the art is short for microprocessor or CPU (*See* Exhibit A, definition of "processor" from www.webopedia.com). The term "microprocessor" is, in turn, known in the art to be a silicon chip that contains a CPU or the like. In the world of personal computers, the terms microprocessor and CPU are used interchangeably. At the heart of all personal computers and most workstations sits a microprocessor. Microprocessors also control the logic of almost all digital devices, from clock radios to fuel-injection systems for automobiles. In addition to bandwidth and clock speed, microprocessors are classified as being either RISC (reduced instruction set computer) or CISC (complex instruction set computer). (*See* Exhibit B, definition of "microprocessor" from www.webopedia.com) Thus, the term processor as is known in the art, refers to a microprocessor or ASIC device suitable for processing instructions. This definition, in turn, indicates that the term "resources within a processor" refers to resources on board a microprocessor or ASIC device. This is backed up by FIGURE 2, which depicts a high-level block diagram of a CPU. This diagram depicts exemplary "resources within a processor" such as reorder buffer 206, load and store buffers etc. (See Page 8, Lines 9-14)

Thus, the invention of Claims 1 generates resource identifiers which correspond to resources within the execution path of a processor (such as a reorder buffer entry). Once an instruction has been fetched, the processor resource requirements of an instruction may be determined, and based on the requirements of the instruction the resource identifier selector may select one or more of the resource identifiers for allocation to the instruction.

Nakagawa does not relate to allocation of resources within a processor. Instead, Nakagawa relates to program execution control devices for storing instructions to addresses of memory, wherein these addresses are sequentially designated in accordance with an M series pseudo-random number sequence in the order of program addresses of each instruction. The instructions may then be fetched from memory using a feedback shift register for generating pseudo-random numbers in accordance with the M series pseudo-random number sequence and read from the instruction memory according to addressing based on the generated pseudo-random number. (*See* Nakagawa Col. 3, Line 9 – Col. 4, Line 26) These instructions are read from the instruction memory into a processor for execution. Consequently, Nakagawa deals with the accessing of resources external to a processor, namely, instruction memories, through pseudo-random number based addressing; not the allocation of resources within a processor as recited by Claim 1.

Similarly, Claim 1 recites a sequence generator that generates one or more resource identifiers, each resource identifier corresponding to one of the resources within the processor, As discussed above, Nakagawa designates addresses of a program memory not resources within the processor. Nakagawa generates program addresses corresponding to locations in an instruction memory based on the pseudo-random number generator, not resource identifiers corresponding to one of the resources within the processor, as does the sequence generator recited in Claim 1. Consequently, the pseudo-random number generator of Nakagawa cannot function as the sequence generator of Claim 1.

Accordingly, as Nakagawa does not disclose all the limitations of Claim 1, Applicant respectfully requests the withdrawal of the rejection of Claim 1. Additionally, as Claims 20, 31 and 38 recite similar limitations to Claim 1, Applicant respectfully requests the withdrawal of the rejection of these claims as well.

Dependent Claims 2-19, 21-30 and 32-37

As dependent Claims 2-19, 21-30 and 32-37 are further limitations on patentable Claims 1, 20 or 31, Applicant respectfully submits that these claims are allowable as well. Therefore, Applicant respectfully requests the withdrawal of the rejection of dependent Claims 2-19, 21-30 and 32-37.

CONCLUSION

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-38. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

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